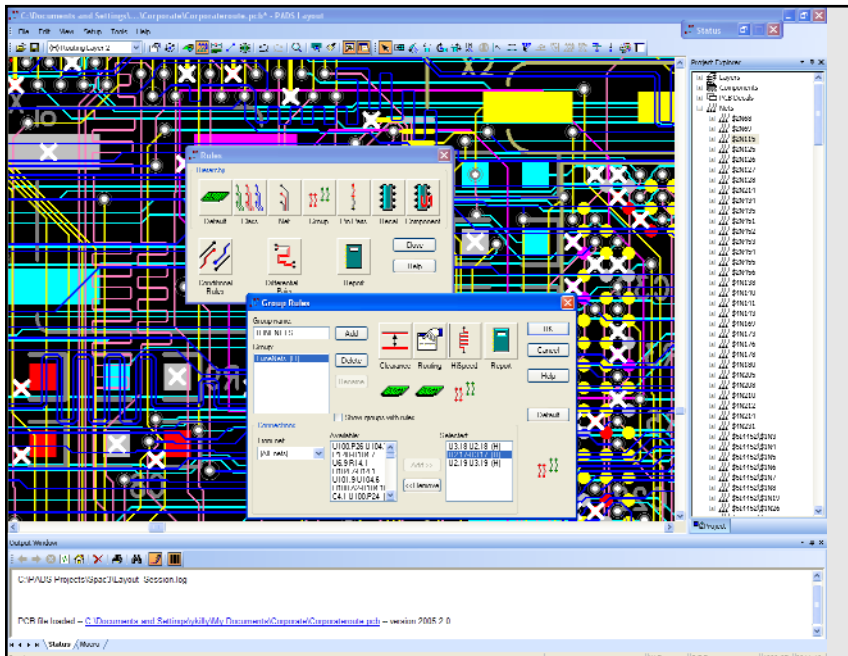


# PADS Layout



The PADS Layout solution combines ease of use with great value and broad technology, making it ideal for complex PCB designs.

## PADS Layout – Meeting Today’s Design Challenges

Reduced headcounts, increased revenue expectations, and ever-shorter market windows make efficiency and value the two “must-haves” of the modern PCB design market. To keep pace, designers need real power in their layout tools – power that is feature-rich and reliable, yet easy to use and affordably priced.

PADS<sup>®</sup> Layout is the answer. It provides everything you need to complete your toughest designs simply and quickly in a flexible design environment.

PADS Layout integrates seamlessly with the rest of PADS PCB Design Solutions, making PADS Layout part of a complete, integrated flow for design definition, analysis, planning, and layout. Add-on modules for design variant creation, advanced packaging, design-for-test, and more, enable PADS Layout to expand to meet future needs. In addition, PADS Layout offers seamless integration with Mentor Graphics’ HyperLynx<sup>®</sup> tool suite, the industry’s choice for signal integrity accuracy and ease of use.

PADS Layout can also be used standalone, to bring exceptional layout quality from schematics captured with other vendors’ software.

### Major product features

- The standard for Windows-based PCB layout
- Proven, reliable PCB design technology
- Powerful, yet easy to use
- Scalable to fit any requirements
- Advanced capabilities tackle complex design problems with accuracy and ease
- RF design support for complex copper shapes, channel/coplanar waveguide, via fill patterns, and square and chamfered corners for copper

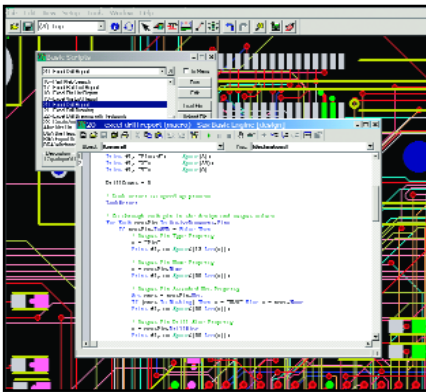
## Overview

PADS Layout is a rich, robust PCB editing environment that provides all the functionality needed to efficiently design and route complex PCBs.

PADS Layout starts with netlist import, reading in all the component and netlist information, component attributes, design rules, and net constraints defined in the schematic. A wizard-driven, shape-creation tool simplifies library component creation and generates accurate land patterns. Component placement is easy and precise, using a combination of manual and automatic tools that allows group placement and component rotation down to a tenth of a degree.

PADS Layout also provides a robust set of manual and interactive routing tools including PADS Router, the shaped-based, any-angle route editor that gives you full control and superior interactive routing in real time.

PADS Layout supports complex split/mixed-plane creation, including custom thermal pad and elaborate cutout support. PADS Layout also audits designs for 100% testpoint coverage and performs essential manufacturability checks before designs are sent out to fabrication.



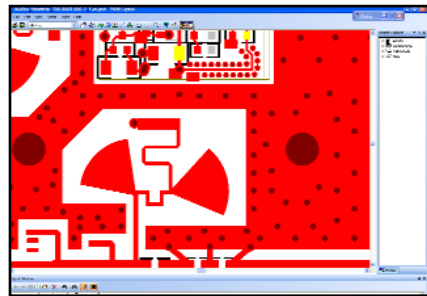
Automation methods allow you to query and modify PADS Layout data structures for better communication with other applications.

PADS Layout also includes automatic and interactive jumper placement, and advanced teardrop and pad-filletting controls for high-density, single- and double-sided boards.

Finally, PADS Layout provides a robust set of menu-driven CAM outputs for all popular manufacturing and test equipment.

## RF Design

Every seat of PADS Layout now has enhanced support for RF and Microwave design, including direct DXF import of complex copper shapes and line geometries into the library editor and/or board editor, via shielding for channel/coplanar waveguide design, auto via fill for any copper shape, and support for chamfered and square corners."



New RF design features include via matrix fill for complex copper shapes.

Only PADS Layout supports RF and Microwave designs through intelligent import of complex copper shapes and line geometries, via shielding for channel/coplanar waveguide design, support for chamfered and square corners, and via matrixing enhancements.

## Automation

PADS Layout combines Object Linking and Embedding (OLE), automation methods, and a Visual Basic engine to provide advanced integration and customization. Extended API commands provide direct access to PADS Layout data structures with other applications, such as Microsoft Excel and other OLE-compliant tools.

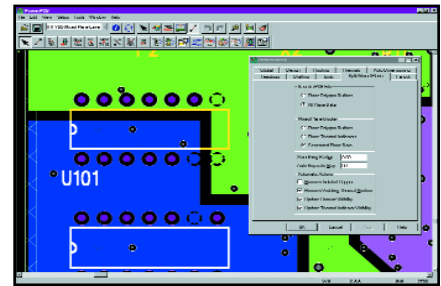
- Cross-probe between applications such as Microsoft® Excel®
- Leverage other EDA and OLE-compliant tools to enhance your design process

- There's a Script Wizard that allows you to leverage automation even if you don't have any programming background.

## Split/Plane Definition

Split/Mixed-Plane operations provide an interactive and automated method for creating complex embedded planes and routes, enabling you to:

- Automatically check connectivity to multiple split-plane areas, ensuring an electrically correct design
- Maintain all design rules, including net-specific and conditional net rules
- Simplify the separation of embedded planes into multiple plane polygons
- Support embedded traces on internal plane layers
- Support positive and negative plane areas.



Split/Mixed-Plane operations ensure connectivity to multiple plane areas.

## Autodimensioning

PADS Layout includes robust dimensioning tools that document the PCB form factor automatically. These tools include datum and standard dimensioning, radius, angle, and leader support, as well as user-defined tolerancing.

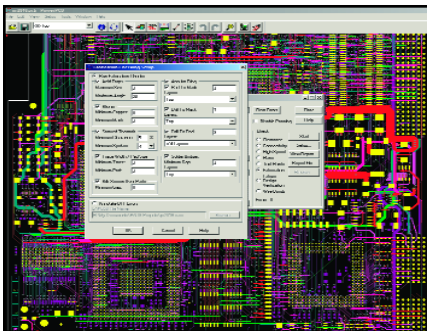
## Online DRC

Design Rule Checks (DRC) enable base and extended rules hierarchy, including layer, class, group, pin pair, and conditional rules. Four modes of operation (prevent, warn, explain, allow) let you choose the degree of system assistance you want as you route.

## Design for Fabrication

PADS Layout includes built-in design-rule checks (DFF Audit) that let you verify designs and correct errors prior to fabrication. By delivering quality layouts to fabrication upfront, you'll avoid respins and costly production delays. You'll also lower the risk of errors being corrected at the fab house and not back-annotated to your design.

- Identify and correct issues that could cause fabrication problems, without leaving the PADS Layout environment
- Check for acid traps, copper slivers, soldermask slivers, traces in a soldermask opening, detection of silkscreen over pads, and more.



With DFF Audit, you can find and fix all rule violations prior to fabrication.

## Assembly Variants

Creates design variants from a single PADS Layout database.

## Analog Design

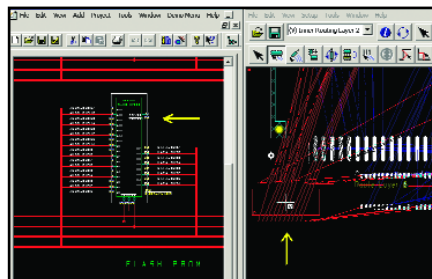
A built-in analog toolkit enables automatic and interactive jumper capabilities and advanced teardrop and pad-filleting controls for high-density,

single- and double-sided boards. By automating typically tedious, manual processes, the analog toolkit saves time and helps ensure that placements will meet your design rules and requirements.

## DxDesigner Link

Provides push-button integration between PADS Layout and DxDesigner™, allowing you to:

- Pass netlists and attributes bidirectionally for seamless schematic-to-layout design synchronization
- Cross-probe between schematic and layout for intuitive component placement and easy identification of critical nets during design reviews.



Integration between DxDesigner and PADS Layout includes crossprobing for intuitive component placement and easy identification of critical nets.

## CAM Outputs

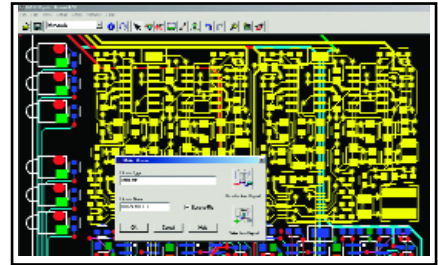
The PCB Editor provides CAM utilities to output DirectCAM, drill data, Gerber, and other standard data-exchange formats.

## Expanded Capabilities

An array of options is available to increase the productivity of your system.

**Physical Design Reuse** – The Physical Design Reuse (PDR) option supports the creation, saving, and placement of physical reuse elements independent of the schematic source. By allowing you to reuse existing, proven circuits, PDR significantly reduces design time. With PDR, you can:

- Save completely routed circuits as reuse elements in a PDR library
- Easily replicate reuse elements to support multi-channel designs, whether the design is newly created or taken from the PDR library
- Use intelligent, element-building technology to create a clone of the initial reuse element and position it on your cursor for placement.

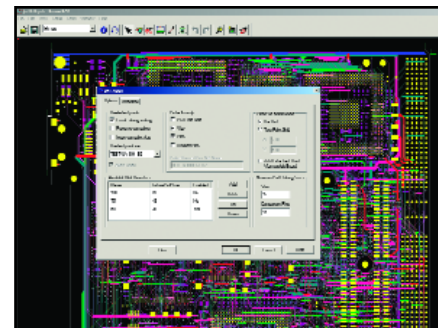


To minimize errors, PDR allows you to replicate 'golden circuits' in new and existing designs.

**Design For Test (DFT)** – DFT Audit enables testpoint assignment and reporting:

- DFT Audit inserts testpoints during normal route passes, converting existing vias and pads to testpoints, or adding necessary testpoints based on your rules. To maximize testpoint coverage, iterative passes can be run with decreasing pad sizes.

- At any time, a comprehensive testpoint coverage report can be generated for design review.



DFT Audit reduces costly design iterations and ensures the In-Circuit Testability (ICT) of your designs before fabrication.

---

*Clusterplacement* – Allows interactive and automatic topographical placement of component groups by function.

*Critical Place & Route (CPR)* – Defines, verifies, and enforces essential pre-placement and pre-layout design rules.

*Database Viewer* – Streamlines communication by sharing PCB design data with the entire design team.

*Advanced Rule Set (ARS)* – Extends the hierarchy of base design rules to include layer, class, group, pin pair, conditional, and differential-pair rule settings. Measures and verifies signal requirements for high-speed layout based on signal routing and board stack-up. ARS is required for high-speed routing.

*IDF Link* – Allows 3D physical information to pass via an IDF file to and from PADS Layout and mechanical engineering tools such as Pro/ENGINEER® and SolidWorks.

*Chip-On-Board (COB)/Advanced Packaging Toolkits* — Automates die-on-substrate design operations using tools such as the die wizard, route wizard, die-flag wizard, wire bond wizard, and advanced post-design report generation.

## PADS Router

PADS Router ships with every seat of PADS Layout. This combination interactive router and autorouter is based on the proven PADS gridless, shape-based technology for highest completion rates and minimal post route rework. Native any-angle. Native any-angle and diagonal routing algorithms accurately and efficiently route high-density designs.

PADS Router follows design rules and net constraints entered at the schematic or PCB level, minimizing post-route checking.

PADS Router follows design rules and net constraints entered at the schematic or PCB level, minimizing post-route checking.

With PADS Router you get:

- Proven interactive and auto routing using "push and shove" and "rip-up and retry" technology for excellent design quality and aesthetics
- A combination of pad-entry controls, same-net clearance rules, and copper sharing that can meet fabrication requirements automatically
- Integrated testpoint routing and post-route auditing to adapt to your existing design-for-test (DFT) process

- True diagonal routing that minimizes trace lengths and design layers
- A context-sensitive, HTML-based Help system.

*High-speed Routing* – PADS Router can be expanded to include capabilities for both interactive and automatic high-speed routing.

- Interactively and/or automatically route complex, length-constrained traces easily and quickly
- Make intelligent routing choices on the fly. The handy "Trace Length Monitor" puts real-time graphical information at your fingertips.
- Handles min/max, matched length, and differential pair traces in real time.

## Operating Systems

Operating Systems – Windows 2000 / Windows XP

Memory Requirements – 512MB minimum 1GB and higher recommended. More memory increases performance.

A complete list of system requirements can be found on our website.

## Summary

Dynamic electronic design environments demand PCB design systems that offer strong technology, reliability, and minimal ramp-up time at an affordable price. PADS Solutions deliver just that, with easy-to-use, integrated full-flow systems that include design definition, front-end simulation, PCB layout, and signal integrity analysis.

Download our software today for a free demonstration, <http://www.mentor.com/padseval>.

## Visit our website at [www.mentor.com/pads](http://www.mentor.com/pads)

Copyright © 2007 Mentor Graphics Corporation. HyperLynx, and PADS are registered trademarks of Mentor Graphics Corporation. All other trademarks mentioned in this document are trademarks of their respective owners.