Embedded Passive Design Solution

System Design

D A T A S H E E T

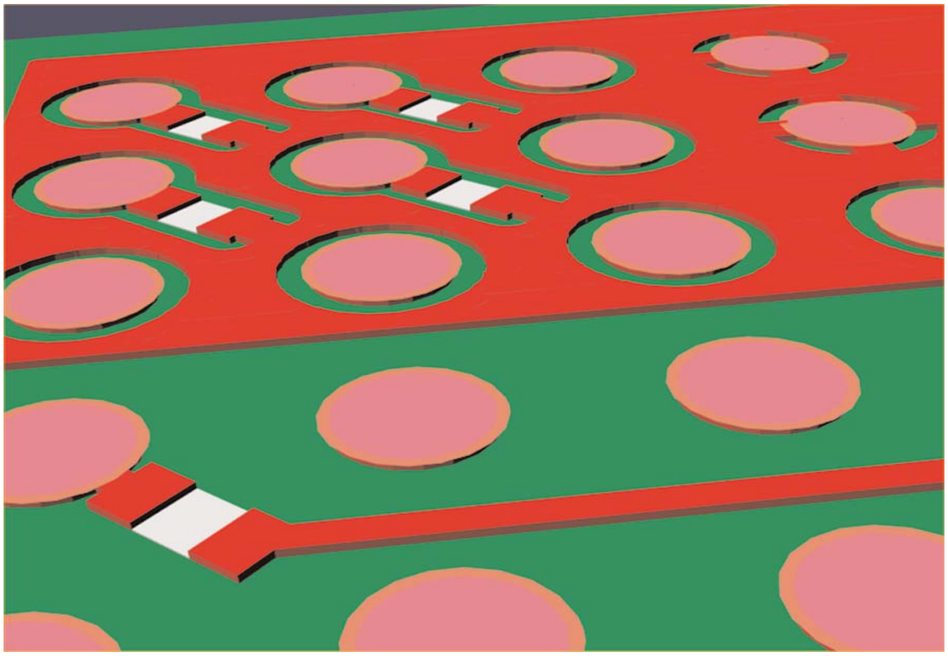

Figure 1: Embedded passives on inner substrate layers can improve performance, lower costs and decrease size.

Major product benefits:

- Mitigate risks through effective management of material data, manufacturing process data and design rules
- Optimize cost and performance through embedded passive design planning
- Cut cycle time through automated embedded passive synthesis and optimization
- Supports both resistor (thick and thin film) and capacitor (mezzanine and printed) technology
- Available in the Board Station XE and Expedition Enterprise design flows

Overview

Today's high density, speed and pin count ICs are requiring an increasing number of supporting resistors and capacitors. Some ICs may require several hundred passives as decoupling capacitors and terminating resistors. Implementing these passives on inner layers (embedded) of the substrate versus as discrete components, can significant reduce the size of the package, improve performance and reduce cost. As a proven technology with its roots in the 1970's, embedded passive technolgoy is being applied in military/aerospace, consumer and industrial designs as means to gain a competitive edge.

Automating the Design Process

In past years, EP's were designed by hand by defining each unique shape, size and material, and storing those in a library for placement in the substrate. This was a very tedious and error prone task that could add weeks to a project. Tedious as there can be literally hundreds of component values, multiple layers and multiple materials giving thousands of part combinations to create and manage with a significant risk of human errors. Now, Mentor Graphics offers a completely automated planning, design, and implementation solution that mitigates the risks, reduces cycle time, and optimizes material utilization and product cost.

This solution enables users to create libraries of suppliers' material characteristics and manufacturing rules. Then using these libraries to perform cost, performance and size tradeoffs, users can make decisions as to which passives to implement in discretes and which to embed. Those to be embedded are automatically synthesized to proper sizes, shapes, tolerances and layers. The passives can then be placed, manipulated and manufacturing data automatically generated. A process that used to take days and weeks, now reduced to hours.

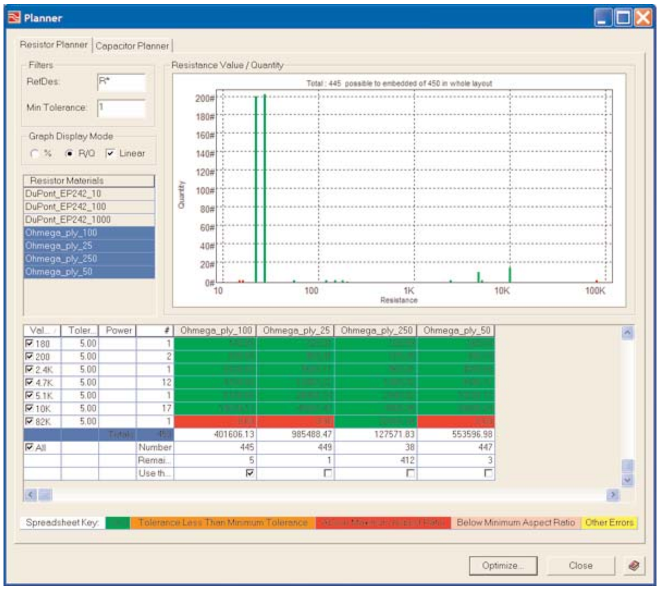

Figure 2: The embedded passive planner and optimizer enables the designer to make cost versus substrate size trade-offs.

Material and Manufacturing Process Library

The first step in the design process is to define manufacturing specific rules and settings as well as material parameters. These parameters are supplied by the embedded material vendors and manufacturers. The Material & Process Editor lets you organize these parameters in an efficient fashion to ensure correct settings for a project. Parameters such as component dimensions relative to required tolerance as well as material and manufacturing cost parameters are managed.

What-if and Tradeoff Analysis

For designs that contain hundreds if not thousands of passives, it is not possible by just looking at a design to determine which passives to embed and what technology, material(s), and manufacturing process will result in the highest performing, smallest size and lowest cost product. The Embedded Passive Planner enables the user to quickly perform what-if scenarios, make those tradeoffs and define a plan for the design of the passives. It will, in seconds, display results for a large set of materials to let you establish which parts to embed, their total component area, and the number of manufacturing process steps required to minimize costs.

Part Synthesis and Optimization

The output of the planner is used to drive synthesis: a process that automatically generates the actual parts for the design. This eliminates the need for pre-designing each passive value, tolerance and shape as a unique entity in a library. You can control what passive shapes are being generated. Resistor shapes include rectangles, top hats, serpentines and folded geometries and for capacitors, screened and mezzanine types. One permutation for each component value, each material and each allowed geometry is generated for the designers review. The designer may now manually select the desired permutation and/or use the automatic optimization to pick the EP's with the smallest component size and to further minimize the number of materials required.

Synthesized parts as passed into the substrate layout function to be placed and routed. During this process, any change that may impact the optimization, such as moving a part to a new layer, will trigger an automatic re-synthesis. Changes with larger impact such as changes to the material or process data will set a DRC flag to help the designer update the design smoothly.

Manufacturing Data

Manufacturing a substrate with embedded passives requires specialized process steps and data. Each technology requires its own specific set of manufacturing data and Mentor's solution supports both artwork generation and data for test and trimming.

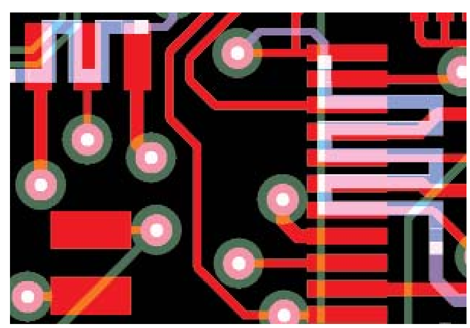

Figure 3: Serpentine resistors can be synthesized to correct value, power and tolerance.

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